DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4 – 6, 9, 11 – 16, and 18 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Henrion (U.S. Pat. No. 5,461,615) (Asynchronous Switching Node Distributing Cells Dynamically to Outputs Constituting an Irregular Group).

2.1 Regarding claim 1, Henrion discloses a method for assigning an address to a node in a network having an arbitrary topology (col. 9, lines 24 – 42 “irregular group”), the method comprising:

assigning a first address to a first node such that the first address includes a description of a path to the first node (Fig. 2; col. 4, lines 24 – 26 “The node can therefore **decorrelate cells having the same destination** but incoming to different inputs of the first stage, since the label selected depends on the input.”; col. 5, lines 25 – 43; col. 6, lines 38 – 50; col. 8, lines 12 – 35; col. 9, lines 24 – 42; col. 3 lines 3 – 7);

assigning a second address to the first node such that the second address includes a description of another path to the first node (Fig. 2; col. 4, lines 24 – 26 “The

node can therefore **decorrelate cells having the same destination** but incoming to different inputs of the first stage, since the label selected depends on the input."; col. 5, lines 25 – 43; col. 6, lines 38 – 50; col. 8, lines 12 – 35; col. 9, lines 24 – 42; col. 3 lines 3 – 7); and

establishing a mapping between plurality of output ports in the network and bits in the first or second address such that a packet, directed to the first address, at a second node in the network is forwarded via an output port on the second node in the network, in response to a specified bit in the first or second address having a specified value (Fig. 2; col. 8, lines 12 – 35 "an output address OPA … includes a plurality of sets of bits each identifying one output of a switching element through which the cell must pass."; col. 5, lines 25 – 43; col. 6, lines 38 – 50).

2.2 Per claim 2, Henrion teaches the method of claim 1 wherein the network is an *optical* network (Abstract "ATM telecommunication networks"; Fig. 1).

2.3 Per claim 4, Henrion teaches the method of claim 1 wherein concurrent bits in the first address map to output ports on the second node (Figs. 1, 2; col. 8, lines 12 – 35; col. 9, lines 24 – 42).

2.4 Regarding claim 5, Henrion discloses the method of claim 4 wherein the map is a one-to-one correspondence (Figs. 2, 3; col. 8, lines 12 – 35; col. 9, lines 24 – 42).

2.5 Per claim 6, Henrion teaches the method of claim 4 wherein each of the output ports on the second node maps to a bit in the concurrent bits in the first address (Figs. 1, 2; col. 8, lines 12 – 35; col. 9, lines 24 – 42).

2.7 Per claims 9, 11 – 16, and 18 – 20, the rejection of claims 1, 2, 4 – 6 under 35 USC 102(b) (paragraphs 2.1 – 2.7 above) applies fully.

Response to Arguments

Applicant's arguments filed 1/20/11 have been fully considered but they are not persuasive.

Applicant argues that "Henrion fails to teach describing paths to the first node"; and that "identifying an output of a node, however, is not the same as identifying or describing a path to the node, as set forth in claim 1."

Examiner disagrees.

Henrion clearly discloses:

assigning a first address to a first node such that the first address includes a description of a path to the first node (Fig. 2; col. 4, lines 24 – 26 "The node can therefore **decorrelate cells having the same destination** but incoming to different inputs of the first stage, since the label selected depends on the input."; col. 5, lines 25 – 43; col. 6, lines 38 – 50; col. 8, lines 12 – 35; col. 9, lines 24 – 42; col. 3 lines 3 – 7);

assigning a second address to the first node such that the second address includes a description of another path to the first node (Fig. 2; col. 4, lines 24 – 26 “The node can therefore **decorrelate cells having the same destination** but incoming to different inputs of the first stage, since the label selected depends on the input.”; col. 5, lines 25 – 43; col. 6, lines 38 – 50; col. 8, lines 12 – 35; col. 9, lines 24 – 42; col. 3 lines 3 – 7); and

establishing a mapping between plurality of output ports in the network and bits in the first or second.

The newly cited portions of Henrion, as well as the previously cited portions of Henrion, teach the limitations that Applicant states are not present.

Allowable Subject Matter

Claim 8 is allowed.

Claims 7, 10, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth R. Coulter whose telephone number is 571 272-3879. The examiner can normally be reached on M - F, 7:30 am - 4 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on 571 272-3868. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth R Coulter/
Primary Examiner, Art Unit 2445

/KRC/